UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,868	03/06/2002	Jeremy D. Dunworth	010482	9970

23696 7590 09/12/2005

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
PERSINO, RAYMOND B	

ART UNIT	PAPER NUMBER
2682	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,868	DUNWORTH ET AL.	
	Examiner	Art Unit	
	Raymond B. Persino	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claim 45 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 43. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). For examination purposes it will be assumed that claim 45 is dependent upon claim 44

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over NELSON et al (US 2002/0075080 A1) in view of ROGERS (US 6,680,655 B2) and POPE (US 6,163,228 A).

Regarding claim 40, NELSON et al discloses a frequency synthesizer comprising: a voltage controlled oscillator (24 of figure 3); a phase locked loop (300 of figure 3) to control a frequency of an oscillating signal of the voltage controlled oscillator; and an amplitude calibration unit (30 of figure 3) to calibrate when the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration) to achieve a desired amplitude for the oscillating signal, the amplitude calibration unit detecting a voltage amplitude (62 of figure 6) of the voltage controlled oscillator and adjusting the voltage amplitude (70 of figure 6) to achieve the desired voltage amplitude until the voltage amplitude falls below a target (see paragraphs 30-37).

However, NELSON et al does not disclose that the voltage controlled oscillator includes a configurable tail current source having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a subset of the switched unit current sources to achieve the desired voltage amplitude, wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target, the target being variably selectable on the basis of a current mode of operation.

ROGERS discloses that the voltage controlled oscillator includes a configurable tail current source (column 7 lines 21-25) having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a subset of the switched unit current sources to achieve the desired voltage amplitude (see Q1-Q6 and 36 in figure 3 and column 4 line 36 to column 6 line 63), wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target (column 8 line 55 to column 9 line 11).

However, ROGERS does not disclose that the target is variably selectable on the basis of a current mode of operation.

POPE discloses that the target is variably selectable on the basis of a current mode of operation (column 1 lines 51-62).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al the VCO mode adjustment of POPE.

ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

POPE's VCO mode adjustment would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 41, see the rejection of claim 40 concerning the subject matter this claim depend upon. NELSON et al further discloses that the voltage controlled oscillator includes additional configurable circuitry that affects the frequency of the voltage controlled oscillator, the frequency synthesizer further comprising a frequency calibration unit (26 of figure 3) to adjust the additional configurable circuitry of the voltage controlled oscillator so as to calibrate the frequency of the oscillator while the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration).

Regarding claim 42, NELSON et al discloses an RF integrated circuit adapted for coupling to an external voltage controlled oscillator comprising: a phase locked loop (300 of figure 3) to control a frequency of an oscillating signal of the voltage controlled oscillator; and an amplitude calibration unit (30 of figure 3) to calibrate when the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration) to achieve a desired amplitude for the oscillating signal, the amplitude calibration unit detecting a voltage amplitude (62 of figure 6) of the voltage controlled oscillator and adjusting the voltage amplitude (70 of figure 6) to achieve the desired voltage amplitude until the voltage amplitude falls below a target (see paragraphs 30-37).

However, NELSON et al does not disclose a configurable tail current source having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a

subset of the switched unit current sources to achieve the desired voltage amplitude, wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target, the target being variably selectable on the basis of a current mode of operation.

ROGERS discloses a configurable tail current source (column 7 lines 21-25) having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a subset of the switched unit current sources to achieve the desired voltage amplitude (see Q1-Q6 and 36 in figure 3 and column 4 line 36 to column 6 line 63), wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target (column 8 line 55 to column 9 line 11).

However, ROGERS does not disclose that the target is variably selectable on the basis of a current mode of operation.

POPE discloses that the target is variably selectable on the basis of a current mode of operation (column 1 lines 51-62).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al the VCO mode adjustment of POPE.

ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

POPE's VCO mode adjustment would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 43, see the rejection of claim 42 concerning the subject matter this claim depend upon. NELSON et al further discloses additional configurable circuitry that affects the frequency of the voltage controlled oscillator, the frequency synthesizer further comprising a frequency calibration unit (26 of figure 3) to adjust the additional configurable circuitry of the voltage controlled oscillator so as to calibrate the frequency of the oscillator while the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration).

Regarding claim 44, NELSON et al discloses an RF integrated circuit adapted for coupling to an external voltage controlled oscillator, the RF integrated circuit comprising: a phase locked loop (300 of figure 3) to control a frequency of an oscillating signal of the voltage controlled oscillator; and an amplitude calibration unit (30 of figure 3) to calibrate when the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration) to achieve a desired amplitude for the oscillating signal, the amplitude calibration unit detecting a voltage amplitude (62 of figure 6) of the voltage controlled oscillator and adjusting the voltage amplitude (70 of figure 6) to achieve the desired voltage amplitude until the voltage amplitude falls below a target (see paragraphs 30-37).

However, NELSON et al does not disclose that the voltage controlled oscillator includes a configurable tail current source having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a subset of the switched unit current sources to achieve the desired voltage amplitude, wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target, the target being variably selectable on the basis of a current mode of operation.

ROGERS discloses that the voltage controlled oscillator includes a configurable tail current source (column 7 lines 21-25) having a number of switched unit current sources; wherein the configurable tail current source adjusts the voltage amplitude of the voltage controlled oscillator by activating a subset of the switched unit current sources to achieve the desired voltage amplitude (see Q1-Q6 and 36 in figure 3 and column 4 line 36 to column 6 line 63), wherein the activating involves de-activating switched unit current sources in discrete steps until the voltage amplitude falls below a target (column 8 line 55 to column 9 line 11).

However, ROGERS does not disclose that the target is variably selectable on the basis of a current mode of operation.

POPE discloses that the target is variably selectable on the basis of a current mode of operation (column 1 lines 51-62).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the voltage detection/correction scheme of ROGERS in the circuit of NELSON et al the VCO mode adjustment of POPE.

ROGERS's detection/correction scheme is advantageous in for use in monolithic implementations since it automatically compensates for variations in load resistance, process parameters and component tolerances without requiring expansive manual adjustments at the board level.

POPE's VCO mode adjustment would result in reduced power consumption thus extending battery life of wireless devices.

Regarding claim 45, see the rejection of claim 44 concerning the subject matter this claim depend upon. NELSON et al further discloses additional configurable circuitry that affects the frequency of the voltage controlled oscillator, the frequency synthesizer further comprising a frequency calibration unit (26 of figure 3) to adjust the additional configurable circuitry of the voltage controlled oscillator so as to calibrate the frequency of the oscillator while the phase locked loop is disabled (see from 66 of figure 6 that loop was not connected during calibration).

Response to Arguments

3. Applicant's arguments filed 6/15/2005 are noted have been fully considered.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Raymond B. Persino whose telephone number is (571) 272-7856. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nick Corsaro can be reached on (571) 272-7876. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Raymond B. Persino RP
Examiner
Art Unit 2682

RP

NICK CORSARO
PRIMARY EXAMINER